Dae Hyun Kim

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Education

10/06 – 05/12 **Georgia Institute of Technology**, Atlanta, GA
- Ph.D. in Electrical and Computer Engineering
- Thesis: Through-Silicon-Via-Aware Prediction and Physical Design for Multi-Granularity 3D Integrated Circuits

08/05 – 08/07 **Georgia Institute of Technology**, Atlanta, GA
- M.S. in Electrical and Computer Engineering

03/98 – 02/02 **Seoul National University**, Seoul, Korea
- B.S. in Electrical Engineering
- Thesis: Design of a frequency synthesizer using sigma-delta modulation

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Experience

08/14 – present **Washington State University**, Pullman, WA
Assistant Professor, School of Electrical Engineering and Computer Science

06/14 – 08/14 **Cadence Design Systems, Inc.**, San Jose, CA
Member of Consulting Staff, IC Digital Group

05/12 – 06/14 **Cadence Design Systems, Inc.**, San Jose, CA
Senior Member of Technical Staff, IC Digital Group

10/06 – 05/12 **Georgia Institute of Technology,** Atlanta, GA
Research Assistant
- Bus routing algorithms for the microarchitecture design
- TSV-aware interconnect prediction models for multi-granularity 3D ICs
- Fast estimation of TSV coupling capacitance
- Studies on the impact of TSVs on the quality of 3D ICs
- Gate-level 3D IC design
- Block-level 3D IC design
- Tape-out of two 3D ICs (3DMAPS-V1 and 3DMAPS-V2)

Spring 2010 **Georgia Institute of Technology,** Atlanta, GA
Teaching Assistant: ECE8823 – "CAD Methodologies for VLSI DFM"
- Designed lab1 (Layout generation and analysis)
- Designed lab2 (Fill synthesis & lithography simulation)
- Designed lab3 (Simulation of process variation)

01/02 – 02/05 **Samwoo Telecom,** Seoul, Korea
Software Engineer
- Ported CTI windows applications to Linux and Solaris systems
- Developed ARS (Automated Response System) programs
- Developed FAX server programs

Publications – Journal

Accepted **D. H. Kim**, K. Athikulwongse, M. B. Healy, M. M. Hossain, M. Jung, I. Khorosh, G. Kumar, Y.-J. Lee, D. L. Lewis, T.-W. Lin, C. Liu, S. Panth, M. Pathak, M. Ren, G. Shen, T. Song, D. H. Woo, X. Zhao, J. Kim, H. Choi, G. H. Loh, H.-H. S. Lee, and S. K. Lim, "Design and Analysis of 3D-MAPS (3D Massively Parallel Processor with Stacked Memory)," accepted in *IEEE Transactions on Computers (**TC**)*.

2014 **D. H. Kim**, S. Mukhopadhyay, and S. K. Lim, "TSV-Aware Interconnect Distribution Models for Prediction of Delay and Power Consumption of 3-D Stacked ICs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**)*, Vol. 33, no. 9, pp. 1384–1395.

2014 M. Bashir, C.-C. Chen, L. Milor, **D. H. Kim**, and S. K. Lim, "Backend Dielectric Reliability Full Chip Simulator," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (**TVLSI**)*, vol. 22, no. 8, pp. 1750–1762.

Accepted C.-C. Chen, M. Bashir, L. Milor, **D. H. Kim**, and S. K. Lim, "Simulation of System Backend Dielectric Reliability," accepted in *Microelectronics Journal*.

2013 **D. H. Kim**, K. Athikulwongse, and S. K. Lim, "Study of Through-Silicon-Via Impact on the 3D Stacked IC Layout," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems (**TVLSI**)*, vol. 21, no. 5, pp. 862–874.

2012 C.-C. Chen, F. Ahmed, **D. H. Kim**, S. K. Lim, and L. Milor, "Backend dielectric reliability simulator for microprocessor systems," *Microelectronics Reliability*, vol. 52, issue 9–10, pp. 1953–1959.

2012 **D. H. Kim** and S. K. Lim, "Design Quality Trade-off Studies for 3D ICs Built with Sub-micron TSVs and Future Devices," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (**JETCAS**)*, vol. 2, no. 2, pp. 240–248.

2011 M. Cho, C. Liu, **D. H. Kim**, S. K. Lim, and S. Mukhopadhyay, "Pre-bond and Post-bond Test and Signal Recovery Structure to Characterize and Repair TSV Defect Induced Signal Degradation in 3D System," *IEEE Transactions on Components, Packaging, and Manufacturing Technology (**TCPMT**)*, vol. 1, no. 11, pp. 1718–1727.

2011 M. Bashir, L. Milor, **D. H. Kim**, and S. K. Lim, "Impact of Irregular Geometries on Low-k Dielectric Breakdown," *Microelectronics Reliability*, vol. 51, issue 9–11, pp. 1582–1586.

2011 **D. H. Kim**, S. Mukhopadhyay, and S. K. Lim, "Fast and Accurate Analytical Modeling of Through-Silicon-Via Capacitive Coupling," *IEEE Transactions on Components, Packaging, and Manufacturing Technology (**TCPMT**)*, vol. 1, no. 2, pp. 168–180.

2010 M. Bashir, L. Milor, **D. H. Kim**, and S. K. Lim, "Methodology to Determine the Impact of Linewidth Variation on Chip Scale Copper/Low-k Backend Dielectric Breakdown," *Microelectronics Reliability*, vol. 50, issue 9-11, pp. 1341–1346.

Publications – Conference

Jan. 2013 K. Athikulwongse, **D. H. Kim**, M. Jung, and S. K. Lim, "Block-level Designs of Die-to-Wafer Bonded 3D ICs and Their Design Quality Tradeoffs," *18th IEEE/ACM Asia South Pacific Design Automation Conference (**ASPDAC**)*, pp. 687–692.

Oct. 2012 C.-C. Chen, F. Ahmed, **D. H. Kim**, S. K. Lim, and L. Milor, "Backend Dielectric Reliability Simulator for Microprocessor System," *23rd European Symposium on Reliability of Electron Devices, Failure Physics and Analysis* (***ESREF***).

Sep. 2012 **D. H. Kim** and S. K. Lim, "Design Quality Trade-off Studies for 3D ICs Built with Sub-Micron TSVs and Future Devices," *SRC TECHCON Conference*.

Apr. 2012 C.-C. Chen, M. Bashir, L. Milor, **D. H. Kim**, and S. K. Lim, "Backend Dielectric Chip Reliability Simulator for Complex Interconnect Geometries," *50th IEEE International Reliability Physics Symposium (**IRPS**)*, pp. BD.4.1–BD.4.8.

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Mar. 2012 K. Yang, **D. H. Kim**, and S. K. Lim, “Design Quality Tradeoff Studies for 3D ICs Built with Nano-scale TSVs and Devices,” *13th IEEE International Symposium on Quality Electronic Design (**ISQED**)*, pp. 741–747.

Feb. 2012 **D. H. Kim**, K. Athikulwongse, M. B. Healy, M. M. Hossain, M. Jung, I. Khorosh, G. Kumar, Y.-J. Lee, D. L. Lewis, T.-W. Lin, C. Liu, S. Panth, M. Pathak, M. Ren, G. Shen, T. Song, D. H. Woo, X. Zhao, J. Kim, H. Choi, G. H. Loh, H.-H. S. Lee, and S. K. Lim, “3D-MAPS: 3D Massively Parallel Processor with Stacked Memory,” *59th IEEE International Solid-State Circuits Conference (**ISSCC**)*, pp. 188–189.

Jan. 2012 **D. H. Kim**, R. O. Topaloglu, and S. K. Lim, “Block-level 3D IC Design with Through-Silicon-Via Planning,” *17th IEEE/ACM Asia South Pacific Design Automation Conference (**ASPDAC**)*, pp. 335–340.

Nov. 2011 **D. H. Kim**, R. O. Topaloglu, and S. K. Lim, “TSV Density-driven Global Placement for 3D Stacked ICs,” *8th International SoC Design Conference (**ISOCC**)* (invited), pp. 135–138.

Sep. 2011 **D. H. Kim** and S. K. Lim, “A Study on the Impact of Nano-Scale TSVs on 3D IC Designs," *SRC TECHCON Conference*.

June 2011 **D. H. Kim**, S. Kim, and S. K. Lim, “Impact of Nano-scale Through-Silicon Vias on the Quality of Today and Future 3D IC Designs,” *13th ACM/IEEE International Workshop on System Level Interconnect Prediction (**SLIP**)*.

May 2011 **D. H. Kim** and S. K. Lim, “Impact of Through-Silicon-Via Scaling on the Wirelength Distribution of Current and Future 3D ICs,” *14th IEEE International Interconnect Technology Conference (**IITC**)*.

Apr. 2011 M. Bashir, **D. H. Kim**, K. Athikulwongse, S. K. Lim, and L. Milor, “Backend Low-k TDDB Chip Reliability Simulator,” *49th IEEE International Reliability Physics Symposium (**IRPS**)*, pp. 2C.2.1–2C.2.10.

Mar. 2011 T. Song, C. Liu, **D. H. Kim**, J. Cho, J. Kim, J. S. Park, S. Ahn, J. Kim, and S. K. Lim, “Analysis of TSV-to-TSV Coupling with High-Impedance Termination in 3D ICs,” *12th IEEE International Symposium on Quality Electronic Design (**ISQED**)*, pp. 122–128.

Nov. 2010 M. Cho, C. Liu, **D. H. Kim**, S. K. Lim, and S. Mukhopadhyay, "Design Method and Test Structure to Characterize and Repair TSV Defect Induced Signal Degradation in 3D System," *28th IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**)*, pp. 694–697.

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Oct. 2010 M. Bashir, **D. H. Kim**, S. K. Lim, and L. Milor, "TDDB Chip Reliability in Copper Interconnects," *18th IEEE International Integrated Reliability Workshop (**IIRW**)*, pp. 121–124.

Sep. 2010 M. B. Healy, K. Athikulwongse, R. Goel, M. M. Hossain, **D. H. Kim**, Y.-J. Lee, D. L. Lewis, T.-W. Lin, C. Liu, M. Jung, B. Ouellette, M. Pathak, H. Sane, G. Shen, D. H. Woo, X. Zhao, G. H. Loh, H.-H. S. Lee, and S. K. Lim, "Design and Analysis of 3D-MAPS: A Many-Core 3D Processor with Stacked Memory," *23rd IEEE Custom Integrated Circuits Conference (**CICC**).*

June 2010 **D. H. Kim**, Y.-K. Wu, R. O. Topaloglu, and S. K. Lim, "Enabling 3D Integration Through Optimal Topography," *4th IEEE International Workshop on Design for Manufacturability and Yield Workshop (**DFM&Y**)*, pp. 70–73.

June 2010 **D. H. Kim** and S. K. Lim, "Through-Silicon-Via-aware Delay and Power Prediction Model for Buffered Interconnects in 3D ICs," *12th ACM/IEEE International Workshop on System Level Interconnect Prediction (**SLIP**)*, pp. 25–32.

Nov. 2009 **D. H. Kim**, K. Athikulwongse, and S. K. Lim, "A Study of Through-Silicon-Via Impact on the 3D Stacked IC Layout," *27th IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**)*, pp. 674–680.

July 2009 **D. H. Kim**, S. Mukhopadhyay and S. K. Lim, "Through-Silicon-Via Aware Interconnect Prediction and Optimization for 3D Stacked ICs," *11th ACM/IEEE International Workshop on System Level Interconnect Prediction (**SLIP**)*, pp. 85–92.

June 2009 **D. H. Kim**, S. Mukhopadhyay and S. K. Lim, "TSV-aware Interconnect Length and Power Prediction for 3D Stacked ICs," *12th IEEE International Interconnect Technology Conference (**IITC**)*, pp. 26–28.

Oct. 2008 **D. H. Kim** and S. K. Lim, "Global Bus Route Optimization with Application to Microarchitectural Design Exploration," *26th IEEE International Conference on Computer Design (**ICCD**)*, pp. 658–663.

Jan. 2008 **D. H. Kim** and S. K. Lim, "Bus-Aware Microarchitectural Floorplanning," *13th IEEE/ACM Asia South Pacific Design Automation Conference (**ASPDAC**)*, pp. 204–208.

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Teaching experience

Spring 2010 **ECE8823 "CAD Methodologies for VLSI DFM"**
Teaching assistant
- Design and grading of three labs
- An in-class presentation on the derivation of lithography simulation formulas

Conference presentations

[8] "TSV Density-driven Global Placement for 3D Stacked ICs," at *8th International SoC Design Conference (**ISOCC**)*, Jeju, Korea, November 2011.

[7] "A Study on the Impact of Nano-Scale TSVs on 3D IC Designs," at *SRC TECHCON Conference*, Austin, TX, September 2011.

[6] "Impact of Through-Silicon-Via Scaling on the Wirelength Distribution of Current and Future 3D ICs," at *14th IEEE International Interconnect Technology Conference (**IITC**)*, Dresden, Germany, May 2011. (poster presentation)

[5] "Enabling 3D Integration Through Optimal Topography," at *4th IEEE International Workshop on Design for Manufacturability and Yield Workshop (**DFM&Y**)*, Anaheim, CA, June 2010.

[4] "Through-Silicon-Via-aware Delay and Power Prediction Model for Buffered Interconnects in 3D ICs," at *12th ACM/IEEE International Workshop on System Level Interconnect Prediction (**SLIP**)*, Anaheim, CA, June 2010.

[3] "A Study of Through-Silicon-Via Impact on the 3D Stacked IC Layout," at *27th IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**)*, San Jose, CA, November 2009.

[2] "Through-Silicon-Via Aware Interconnect Prediction and Optimization for 3D Stacked ICs," at *11th ACM/IEEE International Workshop on System Level Interconnect Prediction (**SLIP**)*, San Francisco, CA, July 2009.

[1] "Global Bus Route Optimization with Application to Microarchitecture," at *26th IEEE International Conference on Computer Design (**ICCD**)*, Lake Tahoe, CA, October 2008.

Professional Activities

- **Technical Program Committee Member**
  - ACM/IEEE System-Level Interconnect Prediction (SLIP) 2014

• **Guest Editor**
- IEEE Design and Test
    - Special Issue on Advances in 3D Integrated Circuits, Systems, and CAD Tools (July/August 2015)

• **Paper Review**
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)
- IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)
- IEEE Design and Test
- Microelectronics Reliability
- Design Automation Conference (DAC)
- IEICE Electronics Express
- ACM/IEE System-Level Interconnect Prediction (SLIP)

Tape-out experience

• **3DMAPS (3D Massively Parallel Processors with Stacked Memory) V1**
- Spec
    - Two-die stacking (face-to-face)
    - # cores: 64
    - Die footprint area: 5mm x 5mm
    - Process: GlobalFoundries 130nm
    - TSV: 1.2μm-diameter
    - Target frequency: 277MHz
    - Supply voltage: 1.5V
- My design part
    - Built a virtual 64-core Verilog code for initial design space exploration
    - Set up tools
    - Created the LEF file of the register file
    - Synthesized and debugged RTL codes
    - Performed signal routing
    - Fixed antenna rule violations

• **3DMAPS (3D Massively Parallel Processors with Stacked Memory) V2**

- Spec
  - Five-die stacking (two logic dies + three memory dies)
  - # cores: 128
  - Die footprint area: 10mm x 10mm
  - Process: GlobalFoundries 130nm
  - TSV: 1.2μm-diameter
  - Target frequency: 180MHz
  - Supply voltage: 1.5V

- My design part
  - Set up tools
  - Synthesized and debugged RTL codes
  - Designed power/ground network
  - Placed macro blocks, face-to-face communication ports, and dummy TSVs
  - Performed DRC and fixed design rule violations
  - Performed LVS of single cores

Skills

Operating Systems: Windows, Linux, Solaris
Programming Languages: C/C++, VHDL, Verilog, Perl, Pascal, Borland Delphi, Borland C++ Builder, Microsoft Visual C++
CAD Tools
- Cadence: Encounter Digital Implementation System, Virtuoso, RTL Compiler, QRC, Library Characterizer
- Synopsys: Design Compiler, PrimeTime, Raphael
- Mentor Graphics: Calibre DRC/LVS/xRC
- Micro Magic: MAX-3D

Simulation/Design Tools: ADS, SPICE, Sonnet, ModelSim, ActiveHDL
Math Tools: MATLAB, Mathematica
Other Softwares: MS Word, Excel, PowerPoint, Access, MS-SQL
Languages: Korean (native), English (fluent)

Honors and Awards

1999 – 2000 **Seoul National University,** Seoul, Korea
- Scholarship

Dae Hyun Kim

Membership

IEEE Member
ACM Member
SIAM Post-Graduate Member

References

Available upon request