

Design Method and Test Structure to Characterize and Repair TSV Defect Induced Signal Degradation in 3D System

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ABSTRACT

In this paper we present a test structure and design methodology for testing, characterization, and self-repair of TSVs in 3D ICs. The proposed structure can detect the signal degradation through TSVs due to resistive shorts and variations in TSV. For TSVs with moderate signal degradations, the proposed structure reconfigures itself as signal recovery circuit to improve signal fidelity. The paper presents the design of the test/recovery structure, the test methodologies, and demonstrates its effectiveness through stand alone simulations as well as in a full-chip physical design of a 3D IC.

1. INTRODUCTION

The Through Silicon Vias (TSVs) in a 3D stack are the channels for transferring signals between different tiers in a 3D stack [1]. The functionality of a 3D IC strongly depends on the fidelity of signals through TSVs. As the TSV process is not a perfect one, defects can be created while forming the TSVs before bonding (assuming a via-first process [2]) or while bonding different dies together. A short during TSV formation creates a resistive defect through the oxide (Fig. 1). Since the substrate surrounding the TSVs is strongly connected to ground, this result is a low resistive path between the TSV and ground. Such shorts in the TSV will result in partial or complete (defect) degradation of signal quality. When the TSV is driven by a driver, the signal swing and/or slew at the receiver end can vary significantly resulting in either complete or partial signal degradation. Therefore, maintaining the signal fidelity through TSVs is a primary challenge in 3D system integration.

It is imperative that the TSV faults need to be detected during pre-bond or post-bond test [3]. The need for post-bond TSV test is obvious to ensure that faulty 3D ICs are not shipped to the customer. On the other hand, the pre-bond test can help to screen the dies with defects and can help reduce potential yield loss by bonding a faulty die with a good one [4]. As post-bond TSVs behave as a wire in the full system, methods for testing wire defects can be adopted. But pre-bond TSV test has significant challenge [5]. The TSVs are too small for test probe and one cannot afford to include a large number of probe pads for testing. Hence, one need to design in-built test structures that can test the TSVs before bonding to ensure whether a die is defect free. If the degraded signal can be recovered at the receiver end of the TSV, it is possible to “repair” the TSVs with moderate defects while maintaining the required system level signal fidelity and improve the design yield.

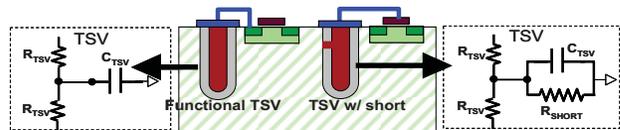


Fig. 1: Schematic illustration of TSV shorts at the pre-bond stage.

The above discussion points to two critical issues in 3D system integration: (a) pre-bond test and characterization of TSVs, and (b) maintaining signal fidelity through TSVs under non-catastrophic defects. This paper, for the first time (to the best of our knowledge), presents an on-line test and self-repair structure and associated design/test methods to address the above two needs of system level 3D integration. The paper makes the following contribution:

- We present a low-overhead digital test structure based on scan flip-flops that detects the pre-bond resistive defects in TSVs and categorizes them in one of the following groups: (a) bad TSVs with complete signal degradation, (b) repairable TSVs with moderate signal degradation and can be recovered with additional circuit, and (c) good TSVs with high signal quality.
- The proposed test circuit reconfigures itself as a signal recovery circuit to repair TSVs with moderate pre-bond or post-bond defects and improve the fidelity of the signals passing through them.
- The efficiency and overhead of the proposed test structure is studied considering full-chip 3D physical design of an example circuit.

2. TEST and SELF-REPAIR STRUCTURE

2.1. Effect of TSV ‘short’ on Signal Quality

Fig. 1 shows a typical scenario where a TSV with short defects is driven by an inverter in one die and the signal is received by another inverter on the second die. The signal degradation at the receiver end is of primary concern for correct functionality of the 3D ICs. Consider variation in the resistance of the short due to variation in the diameter of the short. The voltage at the receiver end can vary significantly resulting in either complete or partial signal degradation. Based on the extent of the signal degradation, we partition the TSVs in three categories. If a low resistance short exists, V_{TSV} will be very low. We refer to this as un-repairable or *bad* TSVs. The TSVs for which V_{TSV} is very high ($>90\% V_{DD}$) are considered to *good* or defect free TSVs. We also define a third category of TSVs, referred to as *repairable* TSVs, which corresponds to shorts with moderately high resistance such that signal degradation is within an acceptable limit (e.g. with 50% of

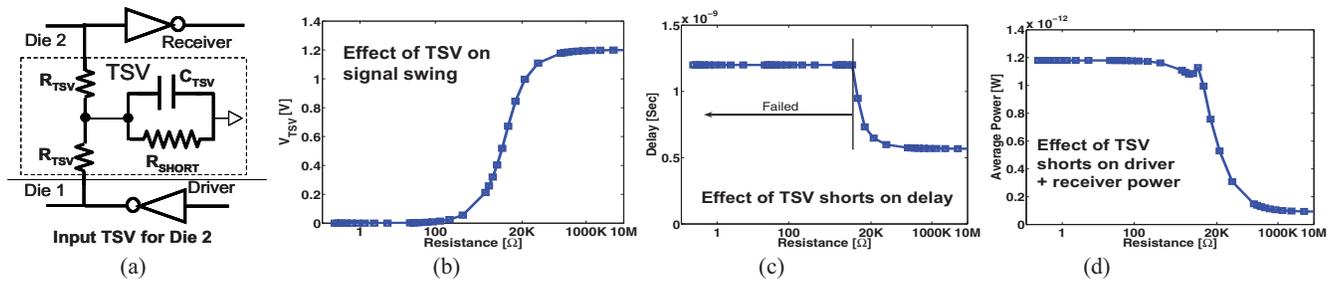


Fig. 2: Effect of TSV short: (a) driver-receiver combination, (b) signal swing, (c) delay, and (d) total (driver + receiver) power.

V_{DD}). During signal propagation through such TSVs, the voltage at the receiver end will make logical transition between ‘0’ and ‘1’ but experience a reduced swing. A lower voltage swing leads to higher noise susceptibility, short-circuit power, and delay at the receiving gate which is illustrated in Fig. 2. As the resistance reduces, signal swing reduces gradually resulting in corresponding increase in signal delay through TSV and average power of the driver/receiver combination. The TSVs with such intermediate resistances of the short belongs to the *repairable* TSVs category. We refer to them as repairable because if the signal swing can be recovered at the receiver end, the TSV will be functioning. If the resistance is very low, the signal fails to make transition.

2.2. Objective of the Pre-Bond Test

After the bonding, the driver and the receiver across a TSV will be at two tiers. Hence, during pre-bond test, our aim is to design a test circuit that can mimic the voltage degradation through the TSVs. But test structure needs to perform this by using all devices in the same tier. The objective of the proposed test structure is to first place individual TSVs in one of three categories during pre-bond test: *bad*, *repairable*, or *good*. If a *bad* TSV exists (assuming non redundant TSVs), the die is detected as a faulty one, not used in bonding, and adds to yield degradation. However, for the repairable TSVs, the test structure reconfigures itself as a signal recovery circuit for post-bond normal operation. This reduces the overall yield degradation at the expense of marginal delay and/or power overhead. For the *good* TSVs, the test structure allows direct signal transfer from the driver to receiver without signal recovery. Note the test structure for repairable TSVs will continue to operate in the recovery mode even after bonding.

2.3. The basic operating principle

Pre-bond Test Mode: A TSV-Test-Inverter (TTI) is connected to each TSV (Fig. 3). During testing the input of the TTI is held low. This forms a resistor divider structure between the PMOS resistance of the TTI-inverter and the resistance of the TSV short. The resistances of the short (R_{short}) and the TTI determines the voltage at the TSV-TTI junction (V_{TSV}). Depending of the value of the R_{short} , the V_{TSV} will vary. V_{TSV} is next compared against a reference voltage and sampled into a scan flip-flop connected to the comparator. The reference voltage is selected such that it represents an “acceptable” signal quality (e.g. $>50\%$ of V_{DD}). The TSVs with low resistive shorts will have values less than the reference voltage while the defect free TSVs will have very high voltage. The scan flip-flops of the TSVs form a scan-chain. The output of the comparator connected to a TSV captures the extent of its short in a digital ‘1/0’ form. At the end of the test, the values stored in the scan flip-flops are scanned out to locate the faulty TSVs. If such TSVs exist the die is categorized as a faulty one. The above test is

performed again but with a higher reference voltage ($\sim 90\%$ of V_{DD}). The scan FFs which indicates faults with this high reference voltage corresponds to *repairable* TSVs.

Signal Recovery during Normal Operation: For the repairable TSVs, the test circuit reconfigures itself to connect the output of the comparator to the input of the logic gates (instead of directly using the TSVs) during normal operation (Fig. 3). The comparator is designed such that during normal operation it functions as level converter circuits and recovers the signal degradation. For the input TSVs the test circuit resides between TSV and the input logic gate.

2.4. Design of the Test and Repair Circuit

Fig. 4 shows the detail circuit schematic of the proposed test structure. Note the scan flip-flops used in the test structure do not function as a flip-flop during regular operation. This allows us to innovate in the design of the proposed structure. The heart of the proposed structure is a differential sense-amplifier based flip-flop. The flip-flop is designed only with the PMOS latch (instead of a CMOS based) to allow it function as a level converter during regular operation. We multiplex the scan input and the TSV input. The select signal of this MUX (SCTRL) controls whether the TSV input or the scan input is applied to input of the differential latch. Since this MUX needs to transfer the TSV voltage during TSV test, we design this using a transmission gate based MUX. The output of this MUX (IN_A) forms the one input of the differential latch. The second input of the differential latch (IN_B) is obtained by multiplexing the reference voltage and inverse of IN_A. This is designed as a tri-state inverter based MUX with V_{ref} as the supply voltage. During scan in or regular operation, the inverse of IN_A is connected to IN_B. During TSV test, the signal TT is high which ensures IN_B is equal to V_{ref} . During scan in or in the signal recovery mode, TT is low which ensures inverse of IN_A is applied to IN_B (Fig. 4).

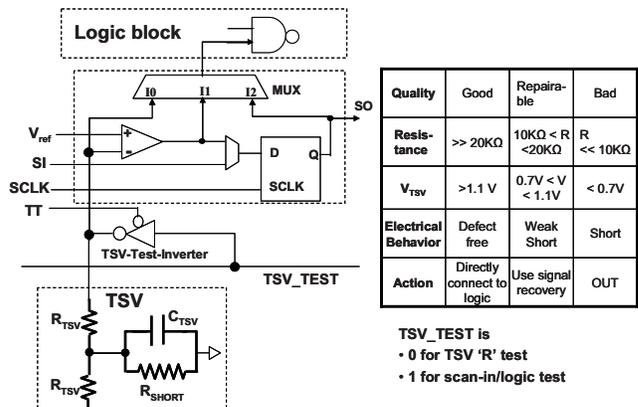


Fig. 3: The basic test structure and characterization policy

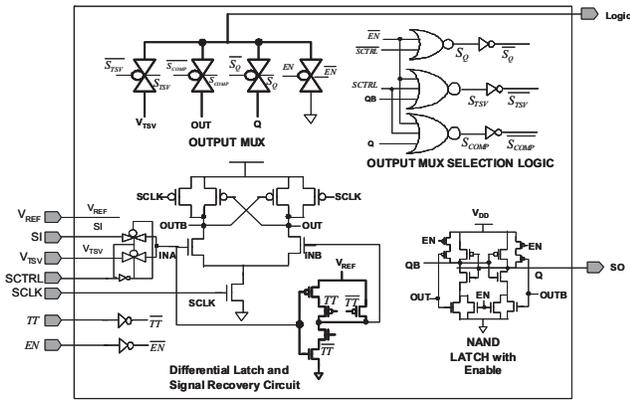


Fig. 4: Circuit schematic of the proposed test circuit

While operating as a flip-flop during TSV test and scan in/out mode, the enable signal (SCLK) of the differential latch is the scan clock signal. However, for signal recovery SCLK is held high so that the circuit behaves as a level converter. This can be achieved by this multiplexing V_{DD} and scan clock. The selection can be achieved using TT and SCTRL. Note the SCLK generation circuit is a global one shared by all test circuits.

The output selection logic is designed to ensure that the logic input is equal to: (a) the output of the scan flip-flop during pre-bond logic test, (b) the output of the comparator for TSVs requiring signal recovery in the operating mode, and (c) directly connected to the output of the TSVs for good TSVs in the operating mode. This can be achieved by multiplexing the three outputs. The control logic for the multiplexer is shown in Fig. 4. Note that select signal that differentiates between scan mode and regular mode is shared by all the test circuits. However, during operation one needs to differentiate between direct TSV connections and comparator connection which is a local signal. We achieve this by re-using the NAND-LATCH connected to the sense-amplifier based flip-flop to store the local requirements of the TSVs. To configure the NAND latches to the proper state we explore two options. First, after pre-bond testing, the requirements for each TSV is stored in a ROM and loaded into the scan flip-flops before starting the operation. Second, the TSV test can be performed while powering up the bonded 3D IC (as a built-in-self-test). The NAND latch is disabled in the recovery mode to ensure the configuration information is not destroyed (Fig.

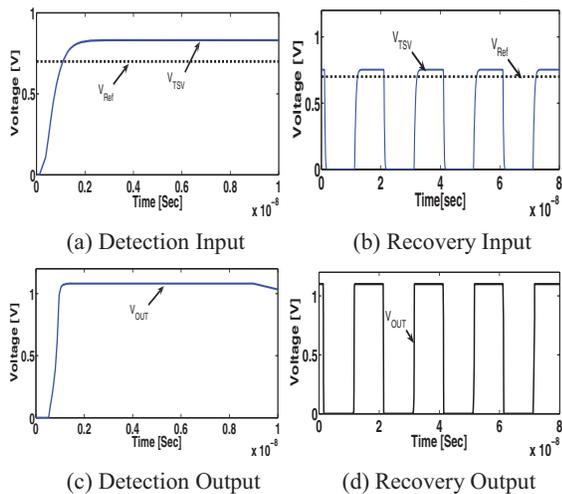


Fig. 5: Waveform of operation

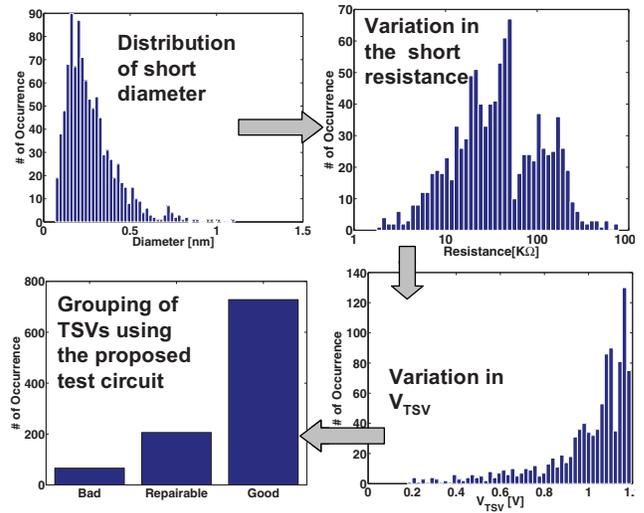


Fig. 6: Statistical simulation results showing the functionality

4). The second option allows the test circuit automatically reconfigures itself as signal recovery circuit during normal operation. In the first option, the reconfiguration is guided by a system level controller.

3. SIMULATION RESULTS

Considering the presence of the differential pair, we first verify the circuit functionality in commercially available IBM90nm CMOS technology. Fig. 5 shows the waveform of the operation of the proposed circuit demonstrating (a), (c) the V_{TSV} detection and (b), (d) signal recovery. It can be observed that the proposed circuit can successfully detect the V_{TSV} value. In the recovery mode, the proposed circuit can successfully recover the low voltage swing. We next consider statistical simulation of variation in the diameter of the short. We consider a log-normal variation in the short diameter (Fig. 6). The resistance corresponding to different short diameters is computed considering copper TSV. As expected, the variation in the short diameter results in a variation in the resistance of TSV shorts. The resistance variation results in a variation in the voltage at the TTI-TSV connection (i.e. V_{TSV}). The proposed test structure successfully detects whether the shorts corresponds to a bad, repairable, or good TSV.

We use FFT256_8 design [6] to demonstrate our experiment on 3D full-chip physical design (Fig. 7). The FFT256_8 is a design with 320K logic gates and 6 metal layers in 45nm technology. The two dies are stacked in a face-to-back fashion with Via-first TSVs. First a min-cut practitioner is used to partition the top level design into two dies. Each cut becomes a pin in each die, which corresponds to a TSV. Next, we place TSVs and standard cells sequentially. Then we place the TSV cells and standard cells together in the first die using the predefined pin locations as constraints. After placement, we change TSV standard cells back to TSV pins so that we can do routing and optimization. For the second die, we first get the TSV landing pad locations from the previous die. With these locations as constraints, we do placement and routing. The following steps are the same as in the first die. After all the designs are done, we perform 3D timing analysis using Primetime. The total number of TSV which we consider is 1444. The area per die is $1.08 \times 1.08 \text{mm}^2$.

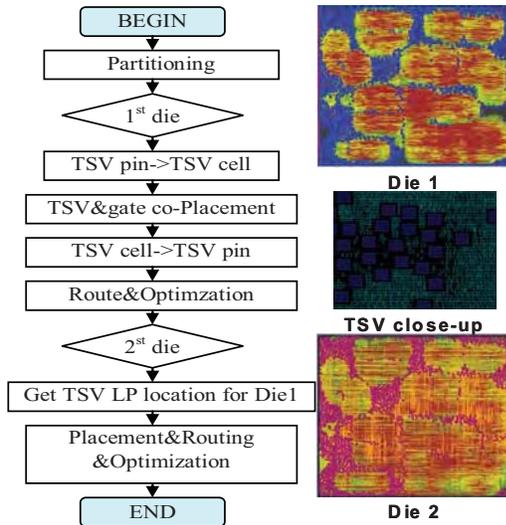


Fig. 7: (left) The 3D Design flow and (right) full-chip layouts of the designed 3D stack

We redesign the proposed test circuit in 45nm PDK technology [7] and verify its functionality. As like its 90nm CMOS counterpart, the 45nm design also performs correct detection and recovery. We next estimate the area, delay, and power dissipation of the proposed test circuit in 45nm node for inclusion into our 3D design flow. The physical area of the proposed design in 45nm is $\sim 21\mu\text{m}^2$. We add this additional cell to each TSV in our 3D design flow to estimate the area overhead. The area overhead of the proposed design was observed to be less than 4% of the total die area when TSV area is $\sim 20\%$ of the die area (Fig. 8a). Next we study the impact of the proposed design on the timing. We first estimate the delay overhead of the proposed design for different short resistances considering presence/absence of signal recovery through SPICE simulation of the proposed design in predictive 45nm node (Fig. 8b). It can be observed that with the proposed circuit delay increases marginally for very good TSVs. This is primarily due to addition of the transmission gate at the input of the logic (for both bypass and recovery mode). But for the repairable TSVs we observe a delay reduction due to improvement of the signal slew. Fig. 8c shows the delay distribution of the different TSV paths for two random instances of the TSV diameters across the chip. As expected insertion of the test circuit results in marginal delay degradation for the TSV paths which has very good TSVs. However, for TSVs with moderate resistance (i.e. repairable TSVs) the path delay marginally

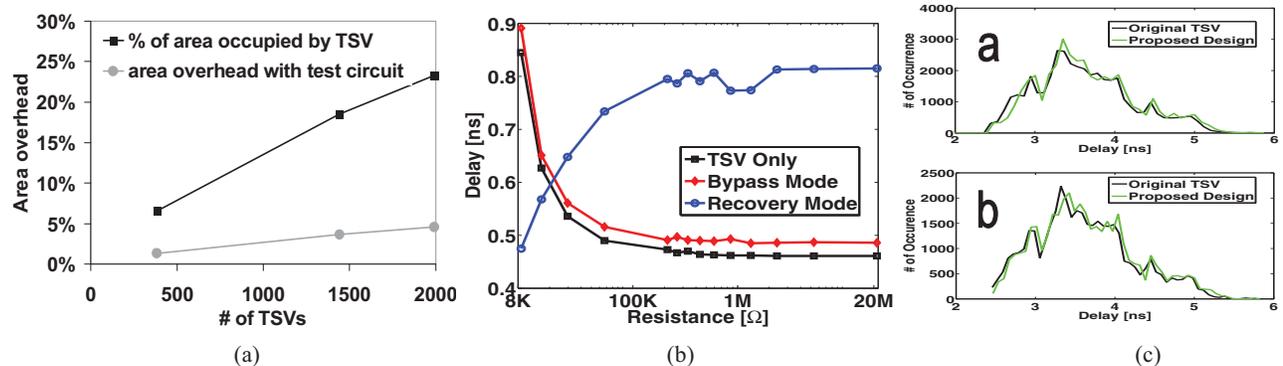


Fig. 8: The area and delay overhead of the proposed structure from system level analysis: (a) the area overhead, (b) the delay overhead of the test circuit in different mode, and (c) path delay distribution for different random instances of the TSV short distributions

reduces from the cases without the proposed recovery circuit. We also perform the power analysis of the proposed test circuit in different mode. The power of the proposed design was observed to be less than microwatt even in the recovery mode.

4. CONCLUSIONS

In this paper we have presented a test structure to detect the effect of TSV defects on the signal quality in a 3D system. The proposed structure can be used at the pre-bond test to detect the TSV defects. Depending on the detected signal quality the proposed structure reconfigure itself to perform signal recovery. The full-chip analysis shows that the signal quality enhancement can be achieved with only moderate area, power, and delay overhead. The future extension of this work will consider the other forms of defects such as weak open in TSVs and TSV-to-TSV resistive bridge.

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