

# TSV-aware Interconnect Length and Power Prediction for 3D Stacked ICs

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**Abstract**— In this paper, we present a new 3D wirelength distribution model which considers the contribution of through-silicon-via (TSV) on wirelength, die area, and power consumption. Since TSVs occupy the device layer together with active devices, the die area increases if TSVs are utilized. This area overhead, which in turn affects the wirelength, worsens due to the large size of TSVs themselves, which is shown to be as large as logic gates themselves. Moreover, the capacitive coupling among TSVs and wires cause non-negligible amount of parasitic capacitance, which worsens power consumption. We present and validate a new 3D wirelength distribution and power consumption model to correctly model the various impacts of TSV.

## I. INTRODUCTION

Since 3D ICs were introduced to overcome the ever-worsening interconnect delay/power problems of 2D ICs, several works have presented wirelength distribution model in 3D ICs [1], [2], [3]. One of their main observations was that the total wirelength, as expected, decreased as the number of dies increased and that the amount of reduction increased as the number of dies increased in the 3D stack. But their wirelength prediction models tend to ignore the area, power, and delay contributions from TSVs themselves and focus more on wires.

TSVs themselves, however, occupy significant bulk and layout space. For example, a  $5\mu \times 5\mu m$  square-shaped TSV occupies  $25\mu m^2$  while a  $1.5\mu \times 1.5\mu m$  gate (= typical in 45nm library) occupies  $2.25\mu m^2$ . This means 90,000 TSVs occupy approximately the same amount of silicon area as one million gates. This observation still holds even if the TSV size is smaller because designers will want to use as many TSVs as possible to decrease wirelength. Therefore, TSV area is not negligible and should be thoroughly investigated during 3D wirelength distribution modeling.

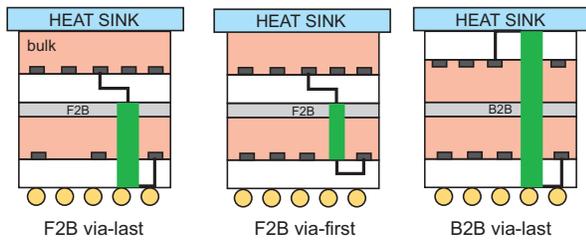


Fig. 1. Bonding style and TSV types. Via-first TSVs occupy bulk and device layer, while via-last TSVs occupy the metal layer in addition. In F2B (face-to-back) bonding, the metal side (= front) of one die is bonded with the bulk side (= back) of another die.

Interconnect power in 3D ICs is also affected by TSVs because of the non-negligible parasitic capacitance caused by TSVs. Figure 2

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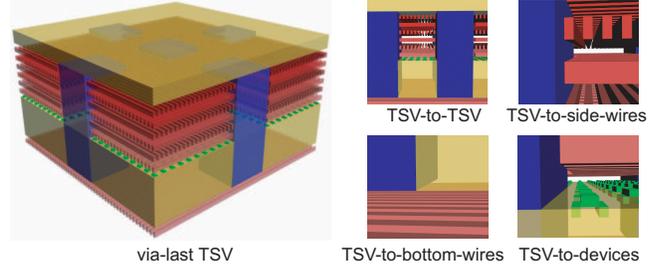


Fig. 2. Parasitic capacitance caused by TSVs that are surrounded by other TSVs and wires

shows various kinds of coupling parasitics caused by TSVs: between TSVs, between TSVs and wires, and between TSVs and devices. These values, according to our calculation, add up to non-negligible values. For example, the capacitance of a  $5\mu \times 5\mu m$  square-shaped and  $50\mu m$ -tall TSV is approximately  $37fF$ , which is similar as the capacitance of a  $400\mu m$ -long wire in 45nm technology. Therefore, power consumption from TSVs should also be considered to correctly compute the total interconnect power.

## II. 3D WIRELENGTH DISTRIBUTION MODELING

The normalized wirelength distribution without consideration of TSV size in [1] can be rewritten as follows:

$$i(l) = \Gamma \cdot M_t[l] \cdot I_{exp}[l] = i_h(l) + i_v(l) \quad (1)$$

$$i_h(l) = \Gamma \cdot I_{exp}[l] \cdot \sum_{v=0}^{N_{DIE}-1} M_z[v] M_S[l - vr] \quad (2)$$

$$i_v(l) = \Gamma \cdot I_{exp}[l] \cdot \sum_{v=0}^{N_{DIE}-1} N_S(N_{DIE} - v) \delta[l - vr] \quad (3)$$

where  $\Gamma$  is a normalization coefficient,  $M_t[l]$  is the number of gate pairs separated by  $l$  gate pitches in 3D,  $M_z[v]$  is the number of die pairs separated by  $v$  vertical pitches,  $M_S[l]$  is the number of gate pairs separated by  $l$  gate pitches in a die,  $N_S$  is the number of gate sockets in a die and  $N_{DIE}$  is the number of dies.  $i_h(l)$  is the distribution of wires whose horizontal length is non-zero (call this  $NPV$  wires) while  $i_v(l)$  is the distribution of wires whose horizontal length is 0 and vertical length is non-zero (call this  $PV$  wires).

$PV$  wires are not affected by TSV insertion because those do not have horizontal components. On the other hand,  $NPV$  wires are affected by TSV insertion as shown in Figure 3 because transistors cannot be fabricated in the TSV locations and TSVs increase silicon area so that the distance of two gate sockets become longer. Therefore,  $i_v(l)$  remains as it is while  $i_h(l)$  should be re-normalized with new functions considering inserted TSVs.  $i_h(l)$  can be written

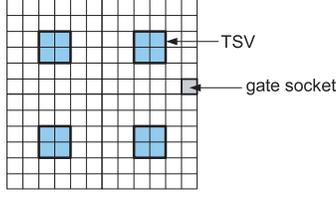


Fig. 3. The so-called “gate socket” grid introduced in [1], which models the placement grid used for wirelength prediction. In our case, each socket contains one gate, while each TSV occupies  $2 \times 2$  grid.

as follows:

$$i_h(l) = \sum_{v=0}^{N_{DIE}-1} i_h(v, l) \quad (4)$$

$$i_h(v, l) = \Gamma \cdot I_{exp}[l] \cdot M_z[v] M_S[l - vr] \quad (5)$$

where  $i_h(v, l)$  is the wirelength distribution of *NPV* wires whose total length is  $l$  and vertical length is  $v$  vertical pitches. Since the vertical length of *NPV* wires does not change while the horizontal length changes by TSV insertion, the total number of *NPV* wires whose vertical length is  $v$  before and after re-normalization should be conserved. This number is computed as follows:

$$N_h(v) = \sum_{l=1}^{2\sqrt{N_S}} i_h(v, l) \quad (6)$$

where  $N_S$  is the number of gate sockets in each die. The new wirelength distribution of *NPV* wires whose total length is  $l$  and vertical length is  $v$  vertical pitches is computed as follows:

$$i_h^*(v, l) = \Gamma(v)^* \cdot I_{exp}^*[l] \cdot M_z[v] M_S^*[l - vr] \quad (7)$$

$$\Gamma(v)^* = \frac{N_h(v)}{\sum_{l=1}^{2\sqrt{N_S}} I_{exp}^*[l] \cdot M_z[v] M_S^*[l - vr]} \quad (8)$$

$$N_S^* = A_{3D}/N_{DIE} \quad (9)$$

where  $\Gamma(v)^*$  is the re-normalization coefficient for *NPV* wires whose vertical length is  $v$  vertical pitches,  $I_{exp}^*[l]$  is the modified expected number of interconnects connecting two gate socket pairs at a distance of  $l$ , and  $M_S^*[l]$  is the modified total number of gate socket pairs at a distance of  $l$ . Then the wirelength distribution for *NPV* wires whose total length is  $l$  is computed as follows:

$$i_h^*(l) = \sum_{v=0}^{N_{DIE}-1} i_h^*(v, l) \quad (10)$$

The final wirelength distribution is computed by adding two distributions for *NPV* wires and *PV* wires as follows:

$$i^*(l) = i_h^*(l) + i_v(l) \quad (11)$$

In this paper, the consideration of TSV impact entails the following consequences: (1) TSVs are 4x large as gates and require two-gate-pitch spacing among them, thereby occupying significant amount of device layer, (2) die area is expanded accordingly to accommodate all gates and TSVs, (3) wirelength distribution is re-calculated accordingly using Equations (4)-(11), and (4) power consumption is re-calculated using TSV parasitic capacitance values and updated interconnect capacitance values.

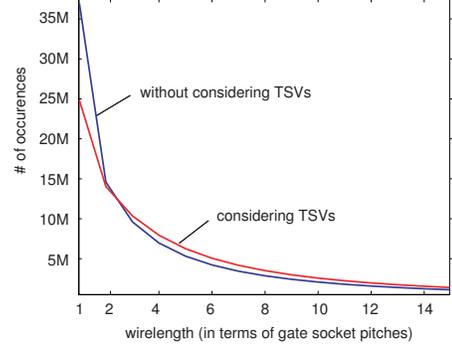


Fig. 4. Comparison of 3D wirelength distribution for short wires. # gates is 40M, and # dies is 2.

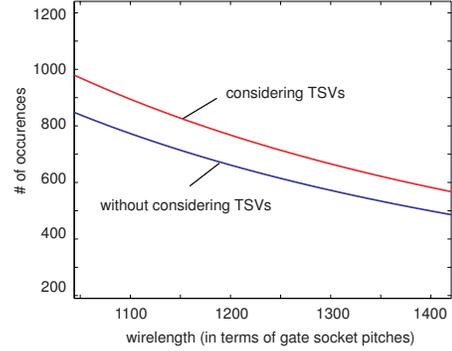


Fig. 5. Comparison of 3D wirelength distribution for long wires. # gates is 40M, and # dies is 2.

### III. EXPERIMENTAL RESULTS

The Rent's constants [1], [2], [3] in our experiments are  $\alpha = 0.75$ ,  $k = 4.0$ , and  $p = 0.75$ . The parameter  $p_{gate}$  that denotes the portion of device area occupied by gate placement is set to 0.75. The die-to-gate-pitch ratio [1], denoted  $r$ , is set to 40 in our experiment. The computation time of average wirelength is 1 second for 40M gates and 4 seconds for 400M gates in Pentium 4 1.8GHz with 1GB memory system. We use 45nm technology, and the gate pitch is set to  $1.37\mu m$ . We use via-first TSV with diameter of  $2.5\mu m$  and spacing of  $5\mu m$ . TSV capacitance was extracted using [4].

#### A. Wirelength Distribution

Figure 4 and Figure 5 show the wirelength distribution (1) without and (2) with the consideration of TSVs. In case of very short wires (= length 1, see Figure 4), the total count becomes lower when TSV impact is considered. This is mainly because, for each gate in the device layer (see Figure 3), there are fewer neighboring sockets with distance 1 due to the TSVs that become placement obstacle. For all other wires, TSVs cause the average wirelength to increase, which is expected since the die area is expanded. In case of medium/long wires (Figure 5), the same trend is observed here, where TSVs cause the average interconnect length for medium and long wires to increase, mainly due to the die area expansion.

Table I shows more details on the impact of TSVs on average wirelength distribution. We report the average wirelength (in terms of gate pitch) for different size circuits under three scenarios: (1) 2D implementation, (2) 3D implementation with no TSV impact, and (3) 3D implementation with TSV impact considered. If the TSV impact is

TABLE I

2D VS 3D AVERAGE WIRELENGTH IN TERMS OF GATE SOCKET PITCHES.  
IN CASE OF 3D, WE COMPARE (1) WITHOUT AND (2) WITH THE  
CONSIDERATION OF TSV IMPACT.

# gates	# dies	2D WL	3D WL		3D WL / 2D WL	
			(1) w/o	(2) with	(1) w/o	(2) with
4M	2	27.97	20.94	24.78	-25.13%	-11.41%
	4	27.97	19.55	23.14	-30.10%	-17.27%
40M	2	49.56	33.98	40.85	-31.44%	-17.57%
	4	49.56	29.27	35.12	-40.94%	-28.91%
400M	2	87.96	56.96	69.14	-35.24%	-21.40%
	4	87.96	45.69	55.36	-48.06%	-37.06%

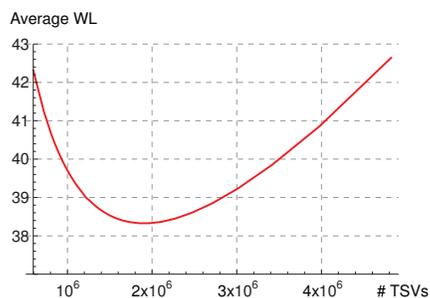


Fig. 6. Relationship between average wirelength in gate socket pitches and the number of TSVs. # gates is 40M, and # of die is 4.

not considered (= therefore unrealistic), the average 3D wirelength is 25% to 48% smaller than 2D counterpart. However, if the TSV impact (= placement obstacle, die area expansion, wirelength increase) is considered, the wirelength saving with 3D reduces to 11% to 37%. Another trend we observe is that the wirelength saving increases with more number of dies in the stack (2 dies vs 4 dies), but the reduction is not close to 2x. This is again mainly due to the TSV impact.

Since the total area occupied by all TSVs in the circuit depends on the TSV size and the number of TSVs, minimization of these two factors becomes important in 3D IC designs. First, TSV size is determined by TSV fabrication technology. This TSV size is expected to decrease as the fabrication technologies advance. Smaller TSVs are always beneficial in terms of area, wirelength, and power costs. Second, TSV count is mainly determined during physical design such as partitioning, placement, and routing. In general, more TSVs mean more wirelength reduction due to the short z-direction connection. However, once the utilization of TSV becomes excessive, wirelength starts to increase again, mainly due to the area impact from TSVs. This trend is shown in Figure 6. In this case, the point of negative return is around 2 million TSVs for this 4-die, gate-level 3D design.

#### B. Interconnect Power

We extended the power model in [5] to add TSV power contribution, which are caused by TSV coupling capacitance and additional wire capacitance from longer wirelength. Table II shows the interconnect power ratio of 3D to 2D. We again compare two cases, where the additional power contributed by TSVs is considered or not. We first observe that in all cases, the power consumption of 3D is lower compared to 2D case (= all numbers are smaller than 1). This is mainly due to the shorter wirelength in 3D in general (see Table I also). We observe that the power saving is more in bigger designs and taller stacks. Second, we see that the impact of TSV power is significant in many cases, where in case of 4M-gate design in 4-die, the power increases by 13% after adding TSV portion. This power

TABLE II

2D VS 3D INTERCONNECT POWER.

# gates	# dies	Interconnect power ratio (3D/2D)	
		(1) w/o TSV power	(2) with TSV power
4M	2	0.89	0.95
	4	0.83	0.96
40M	2	0.82	0.87
	4	0.71	0.80
400M	2	0.79	0.81
	4	0.63	0.68

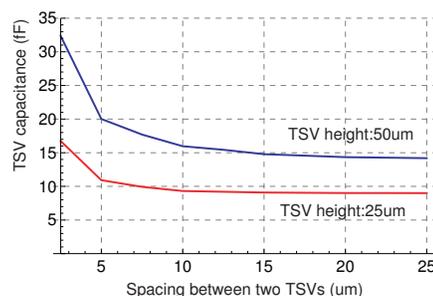


Fig. 7. TSV parasitic capacitance values computed using Synopsys Raphael [4].

overhead is consistent in all cases while the degree varies among each case.

TSV parasitic capacitance depends on the permittivity of the dielectric medium, TSV size and the arrangement of surrounding metal wires and TSVs. Figure 7 shows the TSV capacitances based on various spacing and height. We observe that taller TSVs experience more coupling, while the distance among TSVs can be controlled to reduce the coupling (similar experiments on the impact of surrounding wire variations are conducted but not shown due to space limit). This shows that die-thinning has significant impact on power consumption since the height of TSV is set by the thickness of the dies in the 3D stack. In addition, die thickness also affects the size of TSVs themselves. Thus, thinner dies mean smaller TSVs, which in turn means low parasitic, low delay, and low power consumption. However, die thinning needs to be done carefully while considering various mechanical and electrical properties of the dies.

#### IV. CONCLUSIONS

In this paper, we derived a new 3D wirelength distribution model considering the impact of TSV on area, wirelength, and power. We observed that, mostly due to its size, TSVs cause the average and total 3D wirelength to increase, the overall die size to increase, the capacitive coupling among TSVs and wires to increase, and total power consumption to increase. Thus, design and manufacturing need to be done carefully to consider these impacts.

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